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MergeOptics GmbH M60068PCT

## WHAT IS CLAIMED IS:

- 1. An integrated circuit arrangement on the basis of III/V semiconductors, comprising at least one active component (2) and a multilayer configuration of wiring levels, characterized in that a metallization layer comprising a metal contact (4) of the at least one active component (2) is formed to be a lower one of the wiring levels.
- 2. The integrated circuit arrangement as claimed in claim 1, characterized in that a passivation layer (8) made of a material which has a small relative dielectric constant erl (erl<3) is applied on the metallization layer of the at least one active component (2).
- 3. The integrated circuit arrangement as claimed in claim 1.

  characterized in that an electric resistor is formed in the

  lower wiring level (30) by means of an interruption (7) in the

  metallization layer.
  - 4. The integrated circuit arrangement as claimed in claim 2 or 3, characterized in that a central wiring level (11) is disposed above the passivation layer (8) and covered by another passivation layer (13) made of a material which has a mean relative dielectric constant £r2(£r2>£r1, preferably £r2 ≈ 7).
    - 5. The integrated circuit arrangement as claimed in claim 4, characterized in that an upper wiring level (14) is disposed above the central passivation layer.
- 25 6. The integrated circuit arrangement as claimed in claim 4, characterized in that a capacitive component is formed by means of a section (17) of the central wiring level (11) and a section (18) of the upper wiring level (14).
- 7. The integrated circuit arrangement as claimed in claim 6,
  30 characterized in that the upper wiring level (14) is formed by galvanic deposition of metal.

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- 8. The integrated circuit arrangement as claimed in claim 6 or 7, characterized in that the upper wiring level (14) is constructed at least partly by air bridge technology.
- 9. The integrated circuit arrangement as claimed in claim 1,
  5 characterized in that the at least one active semiconductor
  component (2) is a transistor and a metal contact (4) of the
  collector of the transistor is formed by means of the
  metallization layer.
- 10. The integrated circuit arrangement as claimed in claim 4 and any one of claims 5 to 9, characterized in that at least one microstrip conductor is formed by means of the lower, the central, and the upper wiring levels (30, 11, 14).
- 11. The integrated circuit arrangement as claimed in claim 1, characterized in that waveguides are formed on the lower and/or the central and/or the upper wiring levels (30, 11, 14).

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## Abstract of the Disclosure

## Integrated circuit arrangement

The invention relates to an integrated circuit arrangement on the basis of III/V semiconductors, comprising at least one active component (2) and a multilayer configuration of wiring levels. A metallization layer comprising a metal contact (4) of the at least one active component (2) is formed to be a lower one of the wiring levels. In this manner metallization layers which normally are used only for metal contacting of the components can be incorporated in the wiring of the integrated circuit arrangement.

(Fig. 1)

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